IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Klaus Florian Schuegraf et al.	Examiner: Ori Nadav, Ph.D.
Serial No.:	08/902,809	Group Art Unit: 2811
Filed:	July 30, 1997	Docket: 303.278US1
Title:	SELECTIVE SPACER TO PREVENT METAL OXIDE FORMATION DURING POLYCIDE REOXIDATION	

#26 Appeal Brief T. Young 8-15-00

APPEAL BRIEF TO THE BOARD OF PATENT APPEALS AND INTERFERENCES OF THE UNITED STATES PATENT AND TRADEMARK OFFICE

BOX AF
Commissioner for Patents
Washington, D.C. 20231

Sir:

Appellants' Brief on Appeal

This brief is presented in support of the Notice of Appeal, filed on 2 June 2000, from the Final Rejection of claims 23-31 and 36-44 of the above identified application, as set forth in the Final Office Action dated 2 February 2000. Claims 23-31 and 36-44 remain for consideration.

The Appeal Brief is filed in triplicate. The requisite fee of $300.00 as set forth in 37 C.F.R. § 1.17(c) is enclosed. The appellant reserves the right to submit a request for an oral hearing at a later time. Although other fees are not expected, the appellant authorizes the Examiner to charge or credit Deposit Account 19-0743 as necessary. The appellant respectfully requests reversal of the Examiner's rejections of the pending claims 23-31 and 36-44.

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Real Party in Interest

The present application has been assigned to Micron Technology, Inc., a Delaware corporation doing business at 8000 So. Federal Way, Boise, ID 83707, in an assignment recorded on February 13, 1998 (Reel/Frame 8986/0225).

Related Appeals and Interferences

There are no other appeals or interferences known to the appellant which will have a bearing on the Board's decision in the present appeal.

Status of Claims

Claims 23-31 and 36-44 are pending and are all presently rejected. Claims 23-31 and 36-44 are the subject of the present appeal, and are reproduced in the Appendix.

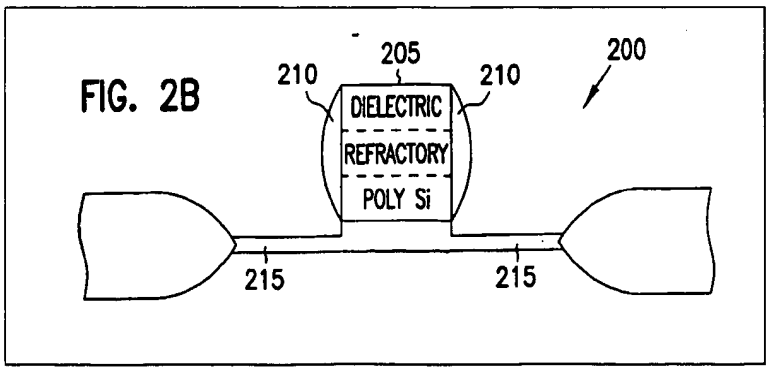
Status of Amendments

No Amendment has been filed subsequent to the Final Office Action dated February 2, 2000.

Summary of Invention

The present invention relates to an electronic device having an electrode on a layer of oxide, and a spacer deposited only on the electrode and not on the oxide.

In one embodiment of the present invention, an electronic device has a patterned electrode 205 on an area 215. Page 4, lines 21-27, Figure 2A. A spacer 210 is deposited only on the electrode 205 and not on the area 215. Page 4, lines 24-27, Figure 2B:



The area 215 is free of deposition due to an incubation time difference 130 between the deposition of spacer materials on polysilicon 110 and the deposition on oxide 120. Page 4, lines 7-9, Figure 1. The spacer 210 comprises silicon nitride or an amorphous silicon film. Page 4, lines 27-28. The electrode 205 comprises polysilicon, a refractory metal, and a dielectric. Page 4, lines 22-23. A polycide reoxidation 220 results in a smile 225. Page 5, lines 3-6, Figure 2C. The electrode 205 may also comprise undoped silicon. Page 5, lines 12-13, Figure 2D.

Issues Presented for Review

I. Were claims 23-31 and 36-44 properly rejected under 35 U.S.C. § 112, first paragraph?

II. Were claims 26-31, 36-41, and 44 properly rejected under 35 U.S.C. § 112, second paragraph?

III. Were claims 23, 25-27, 29, 30, 36, 38, 42, and 44 properly rejected under 35 U.S.C. § 103 as being unpatentable over Ho et al. (U.S. Patent No. 5,364,804, Ho) and Keller et al. (U.S. Patent No. 5,707,898, Keller) in view of Manning (U.S. Patent No. 5,804,838) or McLevige (U.S. Patent No. 4,711,701)?

IV. Were claims 24, 28, 31, 37, 39-41, and 43 properly rejected under 35 U.S.C. § 103 as being unpatentable over Ho, Keller, and Manning or McLevige as applied above, and further in view of Gonzalez (U.S. Patent No. 5,608,249)?

Grouping of Claims

Claims 23-31 and 36-44 stand together for purposes of this appeal.

Argument

I. Rejection of claims 23-31 and 36-44 Under 35 U.S.C. § 112, first paragraph

A) The Applicable Law

The Federal Circuit has addressed the sufficiency of a disclosure in *Vas-Cath Inc. v. Mahurkar,* 19 USPQ2d 1111 (Fed. Cir. 1991). The written description requirement of 35 USC § 112 "comes into play where claims not presented in the application when filed are presented thereafter." *Vas-Cath,* 19 USPQ2d at 1114. The court then stated the standard for compliance with the written description requirement:

> "Although [the applicant] does not have to describe exactly the subject matter claimed,.....the description must clearly allow persons of ordinary skill in the art to recognize that [he or she] invented what is claimed.....The test for sufficiency of support in a parent application is whether the disclosure of the application relied upon reasonably conveys to the artisan that the inventor had possession at that time of the later claimed subject matter." *Vas-Cath,* 19 USPQ2d at 1116.

and:

> "[t]he applicant must ... convey with reasonable clarity to those skilled in the art that, as of the filing date sought, he or she was in possession *of the invention*. The invention is, for purposes of the "written description" inquiry, *whatever is now claimed.*" *Vas-Cath,* 19 USPQ2d at 1117.

The court concluded that "drawings alone *may* be sufficient to provide the "written description of the invention" required." *Vas-Cath,* 19 USPQ2d at 1117.

It is the disclosure of the application that counts in a question of compliance with the written description requirement:

> "While the meaning of terms, phrases, or diagrams in a disclosure is to be explained or interpreted from the vantage point of one skilled in the art, all the limitations must appear in the specification. The question is not whether a claimed invention is an obvious variant of that which is disclosed in the specification. Rather, a prior application itself must describe an invention, and do so in sufficient detail that one skilled in the art can clearly conclude that the inventor invented the claimed invention as of the filing date sought." *Lockwood v. American Airlines Inc.,* 41 USPQ2d 1961, 1966 (Fed. Cir. 1997).

and:

> "One shows that one is in possession of the invention by describing the invention, with

> all its claimed limitations, not that which makes it obvious ... Although the exact terms need not be used in haec verba ..... the specification must contain an equivalent description of the claimed subject matter. A description which renders obvious an invention for which an earlier filing date is sought is not sufficient." *Lockwood,* 41 USPQ2d at 1966.

Claims originally filed with an application "constitute their own description. Later added claims of similar scope and wording are described thereby." *In re Koller*, 204 USPQ 702, 706 (CCPA 1980).

B) The Rejection of claims 23-31 and 36-44

Claims 23-31 and 36-44 were rejected under 35 USC § 112, first paragraph, because each of these claims recite a layer of oxide. As an example, claim 36 recites an electronic device comprising, among other elements, a first layer of oxide and an electrode on the first layer of oxide. The Examiner contends that the layer of oxide was not described in such a way as to reasonably convey to one skilled in the art that the appellant had possession of the claimed invention at the time the application was filed, and to enable one skilled in the art to make and/or use the invention. The appellant respectfully submits that the specification of the present application, as filed, clearly allows persons skilled in the art to recognize that what was originally described and shown as active area 215 is a layer of oxide, and that the specification satisfies the written description requirement set out in *Vas-Cath* and *Lockwood.*

Disclosure

Original Figures 2A-2D show an electronic device including an electrode 205 over an area 215 with a selective spacer 210 deposited only on the electrode 205 and not on the area 215. The area 215 was originally described as "active area 215" on page 4, line 27 and on page 5, lines 5-6 of the specification. The focus of the description is on the selective spacer 210 which is deposited *only* on the electrode 205 and *not* on the area 215 because of the phenomenon shown in Figure 1. Figure 1 illustrates that a "deposition of spacer materials on polysilicon 110 occurs more rapidly than deposition on oxide 120....The difference in incubation time 130 on dissimilar materials makes selective spacer deposition possible." Specification page 4, lines 8-12. Later it is stated that "Figures 2A-2D show how this incubation time difference 130 can be exploited for

selective spacer deposition." Specification page 4, lines 19-20. With reference to the process: "In the second step, represented in Figures 2B and 2C, a selective spacer 210 is deposited such that the amount deposited on the polysilicon and refractory metal 205 is less than the incubation thickness, leaving the active area 215 free of deposition." Specification page 4, lines 24-27. Looking at Figure 2B one skilled in the art could only conclude that the area 215 is oxide. The use of the term "active area 215" is not incorrect because the oxide covers the "active area" in which the electronic device is being formed. Proceeding with the description: "Once the spacer is deposited, the device undergoes polycide reoxidation....active area 215 and selective spacers 210 are reoxidized." Specification page 5, lines 3-6. The layer of reoxidation, shown as 220 in Figure 2C, implies to one skilled in the art the existence of an original layer of oxide - the area 215.

The original claims also provide support for the area 215 being an oxide layer. In claim 9, line 3, the act of forming an *insulating layer* on a semiconductor wafer is recited before the acts of forming a conductive layer and forming a gate by etching. Claim 11 recites a method of forming a structure for controlling current flow between a source and a drain region in a semiconductor device, wherein the semiconductor device is composed of a semiconductor wafer, an *insulating layer* disposed over the semiconductor layer, and a conductive layer disposed over the *insulating layer*, the method including the step of forming a gate having sidewalls exposing the conductive layer and some portion of the *insulating layer*. One skilled in the art would recognize that, according to claims 9 and 11, the gate is formed over the insulating layer. Oxide is known as the most common insulating layer in semiconductor devices. The claims reciting a layer of oxide are supported by the original claims 9 and 11 according to *In re Koller*.

One skilled in the art looking at the whole specification, with emphasis on Figures 2A-2C and claim 11, would understand that the claimed electronic device is a MOS device. MOS devices such as MOS transistors are defined by a source region and a drain region implanted in a substrate or an epitaxial layer on either side of a gate electrode, the gate electrode being insulated by a layer of gate oxide from a channel region in the substrate between the source and drain regions. The embodiment of the invention described in the application is a gate structure for a MOS device. In Figures 2A-2D one skilled in the art will recognize that the area 215 must be a layer of oxide to be consistent with what is known about gate structures in MOS devices. The

oxide is necessary for MOS devices to function. A source region and a drain region are not shown because they are not necessary to a description of the selective spacer 210 that is deposited on the electrode 205 and not on the area 215.

The Examiner has indicated in several Office Actions that, as one skilled in the art reading the specification, he understands that the area 215 must be a layer of oxide. For example, in the office action dated 9 June 1998, the Examiner rejected claims 13-22 on the ground that "[t]he specification does not describe a layer of silicon oxide deposited on the semiconductor device, thus its function and usefulness are not clear." Paper No. 5, paragraph 12. In response the appellant added new claims 26-31 and 33-41 reciting a layer of oxide. In the office action dated 11 January 1999, the Examiner rejected the new claims 26-31 and 33-41 on the ground that "[t]he specification does not describe a layer of gate oxide under the gate in such a way as to convey to one skilled in the art the function ability of the semiconductor device without a gate oxide." Paper No. 12, paragraph 6. The Examiner made this statement again in Paper No. 16, paragraph 5, Paper No. 19, paragraph 6, and in Paper No. 21, paragraph 6. The Examiner therefore understood that the area 215 is a layer of oxide and that the layer of oxide is necessary for the function of the embodiment of the invention described in the specification. The Examiner thereby demonstrated that the specification is sufficient to support the pending claims under *Vas-Cath* and *Lockwood.*

Active Area

The Examiner stated, in Paragraph 17 of the Final Office Action dated 2 February 2000, paper number 21, that "it is well known in the art that an oxide layer is an insulating layer whereas an active area is a conductive area." The appellant respectfully submits that "active area" is known to have a broader definition than just "a conductive area," and this will be demonstrated with the following remarks.

The appellant attached U.S. Patent No. 5,526,306 to Hikawa et al. (Hikawa) and U.S. Patent No. 5,929,494 to Li to the response filed on April 25, 2000. Li is drawn to a read only memory array and uses the terms "active area" and "active region" in a manner known to those skilled in the art. The term "active area" is defined by the following sentence:

> "This array 5 is defined within a single piece of active area of silicon, which is isolated from other active areas by areas of field oxide." Column 5, lines 34-36.

According to Li the term "active area" refers to everything in a semiconductor device that lies between areas of field oxide. "Active area" and "active region" are used interchangeably and both are used to refer to two different aspects of the semiconductor device between areas of field oxide.

"Active region" is often used to refer to a three-dimensional volume of a silicon substrate in which conduction may take place. This is the meaning referred to by the Examiner in stating that "an active area is a conductive area." Li refers to this meaning in the following statement: "A compact ROM array is formed in a single active region (5)," Abstract, line 1. This meaning is also referred to in Hikawa which defines "active region" as a channel 24 shown in Figure 2, a channel 54 shown in Figure 21, and a channel 74 shown in Figure 26. The channels 24, 54, and 74 are three-dimensional regions of a substrate under gate oxide, and between isolating regions or source and drain regions.

The term "active area" clearly includes more than just the three-dimensional volume of conductive substrate described above, but everything in between the areas of field oxide, including gate oxide and features on the gate oxide. This is expressed in Li in the quote above and in the following clauses:

> "In each of the above two cases, therefore, large amounts of field oxide isolation are required to produce the ROM block. Such areas of field oxide isolation are undesirable because the process of growing field oxide layers causes the field oxide to eat into the active areas thereby reducing their size." Column 2, lines 27-32.
>
> "Well-known photolithography and etch techniques are used to define the active region with photoresist 200 and to remove the silicon nitride at the areas where field oxide is to be grown. Since there is no field oxide within the ROM array, the active region is a single piece of area with the field oxide surrounding it." Column 7, lines 9-16.
>
> "Since the active area is large, wafer cleaning before gate oxide growth is desirable to avoid defects." Column 7, lines 31-32.

It is clear that the "active area" referred to above must include the silicon substrate, the gate oxide, and features above the gate oxide that all lie between areas of field oxide. "Active area" is

used in the sentence about cleaning the wafer to avoid defects in the gate oxide, indicating that the gate oxide is part of the "active area." The quote from column 2 indicates that a growing field oxide eats into active areas that include both a silicon substrate and gate oxide. Also, the ROM array needs a layer of gate oxide and features above it to operate. If "active area" were limited to the definition of the Examiner, the gate oxide and everything above it would be excluded, and this would be inconsistent with the use of "active area" in Li as including the ROM array.

Looking at Figures 2-10 of Li, the field oxide 170 is shown as a thick layer of oxide with a bird's beak shape that can be produced by the known LOCOS process of growing field oxide. In all of the Figures 2-10 a thin layer of oxide extends across the entire active area between the areas of field oxide 170. In Figure 2 a pad oxide 130 covers the substrate 160. In Figures 3 and 4 sacrificial oxide 131 stretches between the areas of field oxide 170 during processing steps. A gate oxide 150 is grown in Figure 5 covering the entire substrate 160 between the areas of field oxide 170, and remains through Figures 6-10. The gate oxide 150 is coextensive with the active area as described by Li, being "isolated from other active areas by areas of field oxide." Column 5, lines 36-37. Therefore, in all of the Figures 5-10 of Li there is a gate oxide 150 that is the only feature that is everywhere the "active area" of Li is.

Li thereby indicates the meaning of the terms "active area" and "active region" as is known to those skilled in the art.

Looking now at Figures 2A-2D of the application, one skilled in the art will recognize the similarity between the area 215 and the gate oxide 150 in Figures 5-10 of Li. One skilled in the art will also recognize the similarity between the birds beak shapes in Figures 2A-2D of the appellant's disclosure and the birds beak shape of the field oxide 170 of Figures 5-10 of Li. Looking at Li and Figures 2A-2D, one skilled in the art would understand that the area 215 is a layer of oxide that is coextensive with an active area in Figures 2A-2D and is isolated from other active areas by birds beak shaped field oxide.

The appellant has also filed selections from two textbooks that use the term "active area" known to those skilled in the art. The selections were attached to the amendment filed April 9, 1999.

The first selection is Neil H. E. Weste & Kamran Eshraghian, *Principles of CMOS VLSI Design A Systems Perspective* (1985), pages 71-72. A thin oxide or thinox mask is described on page 71 as defining where areas of thin oxide are needed to implement devices. The term active area is given as another name for the mask, which is shown on page 72 having rectangular areas defining active areas for an integrated circuit.

The second selection is Lance A. Glasser & Daniel W. Dobberpuhl, *The Design and Analysis of VLSI Circuits* (1985), pages 4, 101-103, 176-179, 182, and 183. On page 4 the active area is described as including "regions of heavily doped single-crystal silicon and transistor gate area." On page 102 the active area device edge is described as being moved by field oxidation. An "active area mask is used to define a region to be blocked from field oxidation." In other words, an active area mask defines active areas and insulating areas of field oxide. Figure 2.23 on page 102 also shows the "bird's beak" shape of field oxide similar to that shown in Figures 2A-2D of the specification. On page 103 it is stated that "[i]n MOS technology, oxide thickness is the primary parameter used to distinguish active (transistor) areas from inactive (field) areas." Here is a direct association between a layer of oxide and an active area of an integrated circuit, the active area being defined by a thickness of the layer of oxide. It is therefore not incorrect to point to a layer of oxide and call it an active area. An active area mask is mentioned again on page 176 as defining "what will eventually be sources, drains, channels, and diffused cross unders." The remaining pages describe and illustrate the role of the active area mask.

Therefore the appellant respectfully submits that the specification of the present application, as filed, clearly allows persons skilled in the art to recognize that the area 215 is a layer of oxide. The specification satisfies the written description requirement set out in *Vas-Cath* and *Lockwood*.

Claims

The Examiner commented on the claims individually.

Regarding claims 23-25, claim 23 recites a semiconductor device comprising, among other elements, an oxide layer, at least one feature over the oxide layer, the feature having a surface and being contiguous with the oxide layer at a boundary, and a spacer covering the surface and terminating at the boundary wherein the spacer is not in contact with the oxide layer.

Claims 24 and 25 are dependent on claim 23. Support for these limitations is found in Figures 2B and 2C and in the specification where it is described that the spacer 210 is deposited on the electrode 205 and not on the area 215. Page 4, lines 25-28.

Regarding claims 25-31 and 36-44, the appellant has demonstrated above that one skilled in the art reading the specification would recognize that the area 215 is a layer of oxide, or gate oxide, and that the electrode 205 is a feature protruding from a boundary with the layer of oxide, which is under the electrode 205. Support for this is found in Figures 2A-2C and in the specification, page 4, lines 19-28.

Reversal of the rejection of claims 23-31 and 36-44 under 35 U.S.C. § 112, first paragraph, is respectfully requested.

II. Rejection of claims 26-31, 36-41, and 44 Under 35 U.S.C. § 112, second paragraph

The appellant has demonstrated in section I of the argument that one skilled in the art would recognize that the area 215 is a layer of oxide, or gate oxide. Each of claims 26-31, 36-41, and 44 recite a layer of oxide that is supported by the specification.

Reversal of the rejection of claims 26-31, 36-41, and 44 under 35 U.S.C. § 112, second paragraph, is respectfully requested.

III. Rejection of claims 23, 25-27, 29, 30, 36, 38, 42, and 44 Under 35 U.S.C. § 103

A) The Applicable Law

"A patent may not be obtained...if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art." 35 U.S.C. § 103(a).

A determination of the obviousness or nonobviousness of claimed subject matter is a legal conclusion based on several factual inquiries. "Under §103, the scope and content of the prior art are to be determined; differences between the prior art and the claims at issue are to be ascertained; and the level of ordinary skill in the pertinent art resolved." Against this background, and in light of secondary considerations, the patentability of the subject matter

under §103 is determined. *Graham v. John Deere Co.,* 148 USPQ 459, 467 (1966).

In comparing the prior art with the claims, courts are required to consider the claimed invention as a whole. *Panduit Corp. v. Dennison Mfg. Co.*, 1 USPQ2d 1593, 1597 (Fed. Cir. 1987). The claims must be interpreted in light of the specification, claim language, other claims, and prosecution history. *Id.*

A combination of two or more prior art references must be supported by a showing of a "teaching or motivation to combine" the references. *In re Dembiczak,* 50 USPQ2d 1614, 1617 (Fed. Cir. 1999). Such a showing of a "teaching or motivation to combine" is necessary to avoid the use of hindsight when combining references. *Dembiczak*, 50 USPQ2d at 1616-17. The "evidence of a suggestion, teaching, or motivation to combine may flow from the prior art references themselves, the knowledge of one of ordinary skill in the art, or, in some cases, from the nature of the problem to be solved." The showing of evidence "must be clear and particular," and "[b]road conclusory statements regarding the teaching of multiple references, standing alone, are not "evidence."" *Dembiczak*, 50 USPQ2d at 1617. A §103 reference must be considered in its entirety, "including portions that would lead away from the invention." *Panduit*, 1 USPQ2d at 1597. A court must consider not only the similarities, but also the "critical differences between the claimed invention and the prior art." *In re Bond*, 15 USPQ2d 1566, 1568 (Fed. Cir. 1990).

B) Rejection of claims 23, 25-27, 29, 30, 36, 38, 42, and 44

Claims 23, 25-27, 29, 30, 36, 38, 42, and 44 were rejected under 35 USC § 103(a) as being unpatentable over Ho et al. (U.S. Patent No. 5,364,804, Ho) and Keller et al. (U.S. Patent No. 5,707,898, Keller) in view of Manning (U.S. Patent No. 5,804,838) or McLevige (U.S. Patent No. 4,711,701). The appellant respectfully submits that this combination of references does not disclose all of the elements recited in the claims. Furthermore, there is no suggestion or motivation for combining these references. The appellant will expand these arguments with respect to claim 36 as an example.

Claim 36 recites an electronic device comprising a first layer of oxide, an electrode on the first layer of oxide, the electrode having sidewalls, and a spacer comprising silicon nitride or an amorphous silicon film deposited only on the sidewalls of the electrode, the spacer extending to

and terminating at a boundary between the first layer of oxide and the sidewalls of the electrode.

Ho is deficient in the following respects. Ho discloses in Figure 9 a layer 26 of oxide on sidewall of a gate electrode:

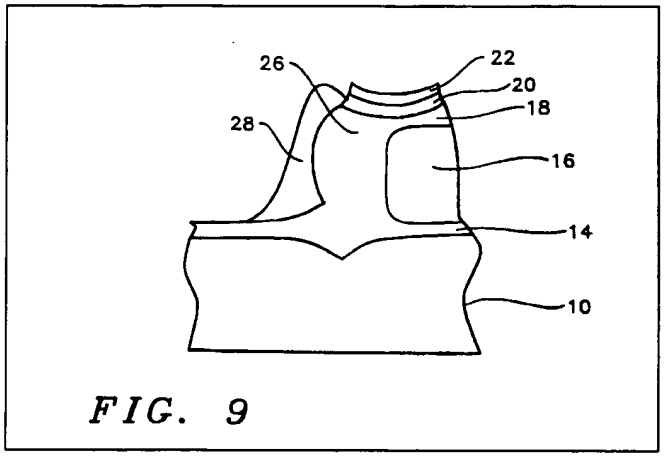


FIG. 9

Ho 5,364,804

Ho also discloses a silicon nitride layer 28 overlaying the oxide layer 26. In column 3, lines 46-48, Ho describes that the purpose of the silicon nitride layer 28 is to provide a more vertical sidewall than the oxide layer 26. Ho does not disclose the spacer comprising silicon nitride or an amorphous silicon film extending to and terminating at a boundary between the first layer of oxide and the sidewalls of the electrode as recited in claim 36. In fact, the very purpose of the silicon nitride layer 28 of Ho is to be in contact with the oxide layer 26 to correct for the non-vertical surface of the oxide layer 26.

Keller does not supply the elements missing in Ho. Keller discloses in Figure 2 a gate construction 16a:

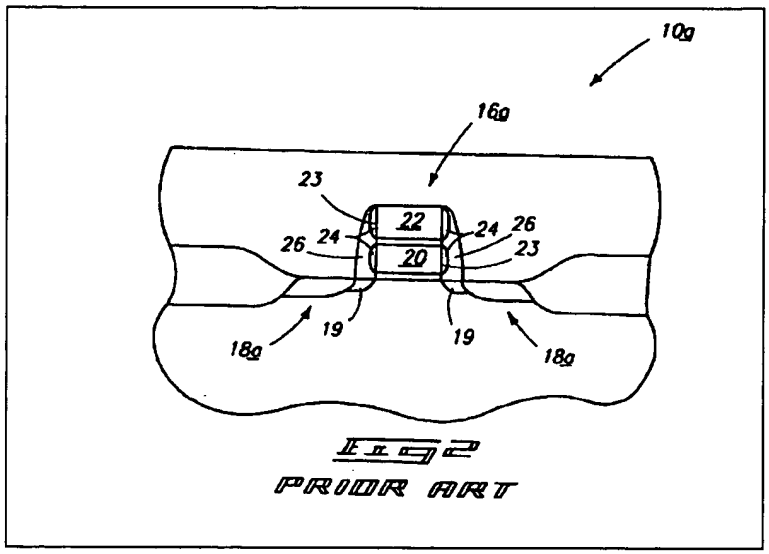


Fig 2
PRIOR ART

Keller 5,707,898

The gate construction 16a is described as including "outer sidewalls 23 having an oxide layer 24 grown thermally thereover." Column 3, lines 2-3. The gate construction 16a further includes "sidewall spacers 26, typically comprising undoped SiO_2" or silicon dioxide. Column 3, lines 20-22. Therefore the layer 24 and the spacers 26 on the gate construction 16a are both oxide, and therefore Keller clearly does not show the spacer comprising silicon nitride or an amorphous silicon film extending to and terminating at a boundary between the first layer of oxide and the sidewalls of the electrode as recited in claim 36.

Manning does not supply the elements missing in Ho and Keller. Manning discloses in Figure 10 silicon nitride spacers 48 and 50 on a silicon material 14 and in contact with a layer of oxide 13:

Manning 5,804,838

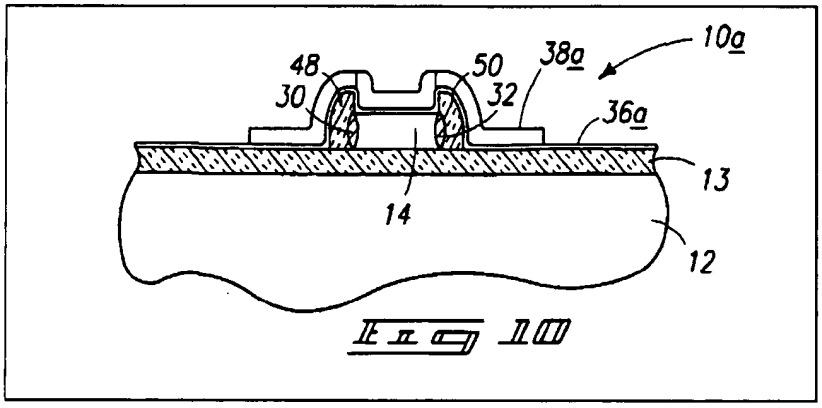


Fig 10

Manning therefore does not disclose the spacer comprising silicon nitride or an amorphous silicon film extending to and terminating at a boundary between the first layer of oxide and the sidewalls of the electrode as recited in claim 36.

Finally, McLevige does not supply the elements missing in Ho and Keller. McLevige discloses in Figure 2d sidewall deposits of SiO_2 64 that are deposited on FPM 42 and an underlying layer of silicon nitride 38:

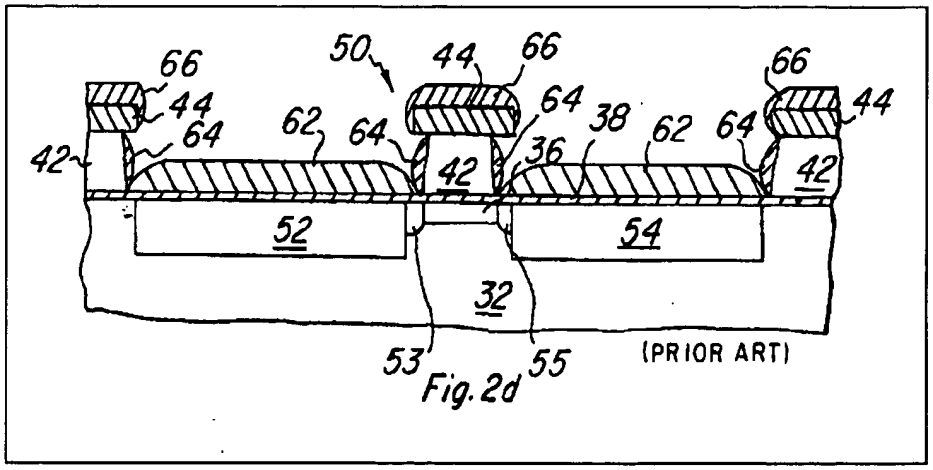


Fig. 2d

McLevige 4,711,701

Figures 3c and 4b of McLevige show a similar deposits. McLevige states in column 5, lines 18-20, that "[i]n the case that the silicon nitride layer is omitted, the silicon dioxide could be replaced by silicon nitride." However, there is no indication that, in making this statement, McLevige is referring to the sidewall deposits of SiO_2 64 and the layer of silicon nitride 38. Therefore, McLevige does not disclose the spacer comprising silicon nitride or an amorphous silicon film extending to and terminating at a boundary between the first layer of oxide and the sidewalls of the electrode as recited in claim 36.

Therefore, none of the applied references disclose the spacer recited in claim 36.

Furthermore, there is no teaching or motivation to combine the references applied by the Examiner as required by *Dembiczak*. The Examiner indicated why the references were combined on page 6 of the Final Office Action dated 2 February 2000:

> " It would have been obvious to a person of ordinary skill in the art at the time the invention was made to deposit a layer of a silicon oxide on a silicon nitride spacer not being in contact with the oxide layer in Ho et al.'s device in order to provide better protection for the device by a method well known in the art. The combination is motivated by the teaching of Ho et al. who point out that spacers can be formed of silicon nitride, and by the teaching of Keller et al. who point out that it is known in the art to form a spacer having a smile effect not contacting a boundary between a feature and an oxide layer (columns 2-3).
>
> Regarding a second oxide spacer having a smile effect, Keller et al. teach in figure 2 that it is known in the art to form a spacer having a smile effect not contacting a boundary between a feature and an oxide layer. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a second oxide spacer having a smile, as claimed." Paper number 21, paragraph 9.

The references themselves teach away from the combination of the Examiner. Ho actually teaches that the purpose of the silicon nitride layer 28 is to be in contact with the oxide layer 26 to correct for the non-vertical surface of the oxide layer 26. The layer 24 and the spacers 26 of Keller are themselves oxide, so they offer no suggestion for the location of a silicon nitride spacer, much less the spacer comprising silicon nitride or an amorphous silicon film extending to and terminating at a boundary between the first layer of oxide and the sidewalls of the electrode as recited in claim 36.

Keller also apparently does not disclose the "smile effect" in columns 2-3, as indicated by the Examiner. Keller also does not disclose "a spacer having a smile effect not contacting a

boundary between a feature and an oxide layer," because the spacers 26 of Keller are themselves oxide.

The Examiner is improperly using hindsight to combine the applied references. Each of the applied references operates without an addition from the others, and there is no suggestion in any of the references for the combination.

Therefore, even as combined, Ho, Keller, and Manning or McLevige do not disclose or suggest all the elements recited in claim 36, or in claim 38 which is dependent on claim 36. Claims 23, 25-27, 29, 30, 42, and 44 recite elements similar to the elements recited in claim 36. For reasons analogous to those stated above with respect to claim 36, and the limitations in the claims, the appellant respectfully submits that claims 23, 25-27, 29, 30, 42, and 44 are not disclosed or suggested by the combination of references put forward by the Examiner.

Reversal of the rejection of claims 23, 25-27, 29, 30, 36, 38, 42, and 44 Under 35 U.S.C. § 103 is respectfully requested.

IV. Rejection of claims 24, 28, 31, 37, 39-41, and 43 Under 35 U.S.C. § 103

Claims 24, 28, 31, 37, 39-41, and 43 were rejected under 35 USC § 103(a) as being unpatentable over Ho, Keller, and Manning or McLevige as applied above, and further in view of Gonzalez (U.S. Patent No. 5,608,249).

Claims 24, 28, 31, 37, and 43 are dependent on the claims discussed above. For reasons analogous to those stated above, and the limitations in the claims, the appellant respectfully submits that claims 24, 28, 31, 37, and 43 are not disclosed or suggested by the combination of references put forward by the Examiner.

Claims 39-41 recite elements similar to the elements recited in claim 36. Gonzalez discloses a gate electrode 18 comprising polysilicon 20, tungsten silicide 22, and silicon dioxide 24. Column 4, lines 61-64. The Examiner did not indicate that Gonzalez disclosed a spacer having the elements missing in the other applied references as discussed above with respect to claim 36. For reasons analogous to those stated above with respect to claim 36, and the limitations in the claims, the appellant respectfully submits that claims 39-41 are not disclosed or suggested by the combination of references put forward by the Examiner.

Reversal of the rejection of claims 24, 28, 31, 37, 39-41, and 43 Under 35 U.S.C. § 103 is respectfully requested.

Conclusion

For the foregoing reasons, the appellant respectfully submits that the Examiner's rejections of claims 23-31 and 36-44 were erroneous. Reversal of those rejections is respectfully requested.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to Box AF, Commissioner of Patents, Washington, D.C. 20231 on **August 2, 2000.**

Tina Pugh _____

Name Signature